RF-Interconnect for Multi-Gb/s Digital Interface Based on 10-GHz RF-Modulation in 0.18μm CMOS

Hyunchol Shin, Zhiwei Xu, M. Frank Chang

High Speed Electronics Laboratory, Electrical Engineering Department
University of California, Los Angeles, CA. 90095, U.S.A.

Abstract — **We present a RF-interconnect (RFI) for multi-Gb/s digital interface based on capacitive coupling and RF-modulation over an impedance-matched transmission line. The RFI can reduce the switching noise coupling greatly and eliminate the dc current dissipation completely over the channel. The improved signal-to-noise ratio enables data transmission with reduced signal swing (as low as 0.2V) and potentially enhanced data speed. A prototype RFI implemented in 0.18μm CMOS demonstrates a maximum data rate of 2.2 Gb/s with 10.5-GHz RF-carrier.**

I. INTRODUCTION

In high speed digital interface, the most popular scheme is a direct-coupled interconnect (DCI) over a matched transmission line as shown in Fig. 1(a), which are actually used in GTL (Gunning Transceiver Logic) or RSL (Rambus Signaling Logic) [1,2]. Those DCIs typically keep high signaling level (0.8V swing plus dc 0.8-1.2V at the terminations) and high output driver current (30mA/pin) to secure sufficient noise margin from the severe digital switching noise. These have been the most limiting factors for the higher data transmission speed. In addition, DCI consume significant dc power during the data transmission, because of the direct coupling. On the other hand, capacitive-coupled interconnect (CCI) (shown in Fig. 1(b)) has been used in high data rate back planes. In spite of the advantages such as no dc-interaction between the nodes, CCI has a limited data rate because it inevitably requires data-encoding/decoding.

Those limitations imposed by DCI and CCI could be overcome by employing the RF/wireless interconnect concept for either clock distribution [3] or signal/data transmission [4,5]. In this paper, we propose to use the RF-modulation on the capacitive coupled interconnect as shown in Fig. 1(c). This RF-Interconnect (RFI) is appropriate for multi-Gb/s digital interface.

II. RF-INTERCONNECT SYSTEM ARCHITECTURE

As shown in Fig. 2, the RFI consists of a transmission line with both ends terminated by Z_o to ground, coupling capacitors (C_c), and direct conversion RF-transceivers. The transmitter (Tx) modulates (up-converts) the baseband signal with the RF-carrier (f_{RF}) before sending it to the channel through the capacitor C_c. The receiver (Rx), on the opposite end, demodulates (down-converts) the signal with the same f_{RF} to the baseband. The RF-modulation is used to enhance the coupling efficiency of the baseband signal. Direct conversion Tx/Rx architecture is selected to minimize the circuit complexity and power consumption.

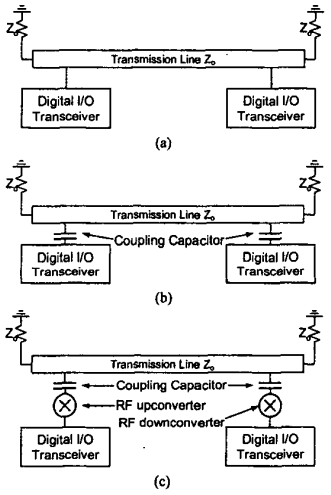

Figure 1. High speed digital interconnect architectures: (a) Direct-Coupled Interconnect (DCI), (b) Capacitive-Coupled Interconnect (CCI), (c) RF-Interconnect (RFI)

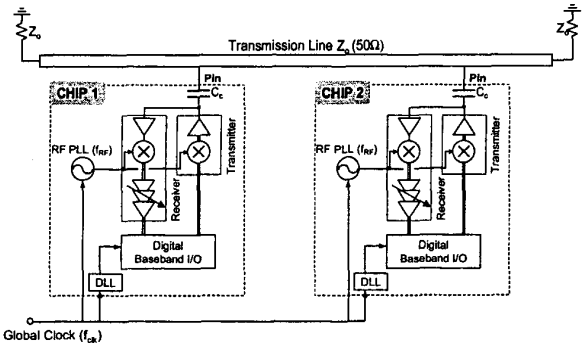

Figure 2. RF-Interconnect system architecture

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We first analyze RFI channel's noise immunity capability. The transmission line under investigation has 20 I/Os (or dropouts) evenly distributed across its 10-cm long channel as illustrated in Fig. 3. Both ends of this line are terminated by its characteristic impedance Z_o (50Ω) on a 15mil thick substrate with dielectric constant of 2.2. The input impedance of each dropout is assumed as $20\times Z_o$. Fig. 4 calculates the high pass (HP) transmission characteristic from one I/O point to another, assuming C_c ranged between 50 fF to 200 fF. It shows a cut-off frequency near 4 GHz when choosing C_c= 50 fF. This characteristic reduces the switching noise coupling near the clock frequency (f_{clk}) while passing the modulated data around the carrier frequency (f_{RF}). Given f_{RF}=10GHz and C_c=50fF, the switching noise around f_{clk}=1GHz is suppressed by 17.5dB. Beyond that, both ends of the RFI channel are firmly terminated to the true ground (versus DCI connected to regulated dc voltages (0.8~1.2V)) through termination resistors Z_o, and the RFI carries no dc signal component on the channel. Both of these arrangements lead to a much quieter channel.

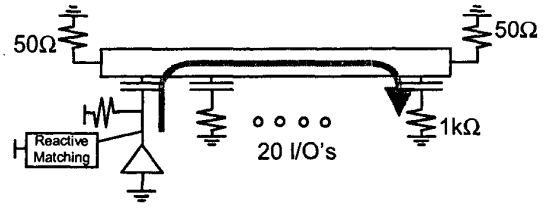

Figure 3. RF-interconnect channel environments with 20 I/O's

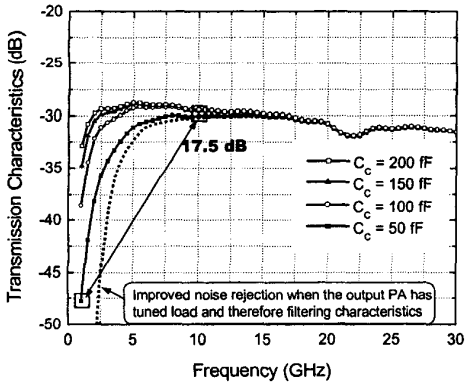

Figure 4. Transmission characteristics of RFI with 20 I/O's

In addition, parasitic inductance of bond wires and package lines causes *di/dt*-ringing to the DCI baseband output signal. The same inductance now becomes part of the matching load for the intended RFI output driver because the desired signal has been up-converted by the carrier f_{RF}. The reactive impedance matching can maximize the power transfer to the channel and further suppress the noise coupling by the filtering characteristic of the output load at f_{RF} as illustrated by the dashed curve in Fig. 4. BPSK (binary phase shift keying) is employed in RFI as a modulation scheme to avoid LO carrier feedthrough in the transmitter and remove the dc-offset in the receiver. An iso-synchronous detection scheme can be used to demodulate the BPSK data by using a 4-phase RF PLL.

III. DESIGN AND IMPLEMENTATION

The prototype chip architecture is given in Fig. 5. Although the ultimate goal for RFI is to realize inter-chip interconnect through a matched transmission line, this prototype is designed to communicate within a chip as the first step of demonstration. Since the transmission distance is short, the output driver and the input pre-amplifier are not included.

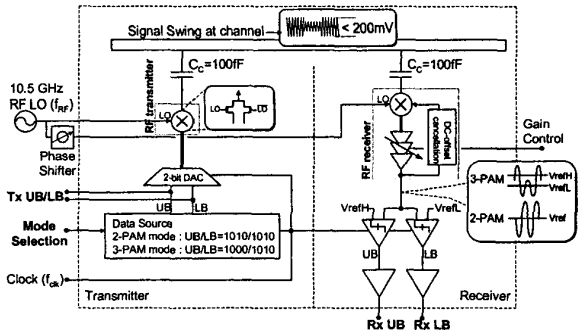

Figure 5. Prototype chip architecture for RFI demonstration

A balanced passive switching mixer is designed for the up-conversion in Tx. A Gilbert-cell down-conversion mixer and a baseband amplifier are designed for Rx. To remove dc-offset in the Rx, an offset cancellation feedback circuit is included as shown in Fig. 6, which can operate either in closed-loop or open loop. The baseband amplifier (Fig. 7) provides a variable voltage gain of 14dB ~ 24dB in order to compensate any unexpected transmission loss. The gain variation is achieved by changing the effective width of the differential pairs of M2,3 and M4,5, which is actually controlled by the steering current thru M1. No inductors are used as loads in Rx to support high baseband data rate. The MIM coupling capacitors of 50 fF are realized with an area of 220μm^2. The RF-modulated signal amplitude is designed as ± 0.1V on the channel.

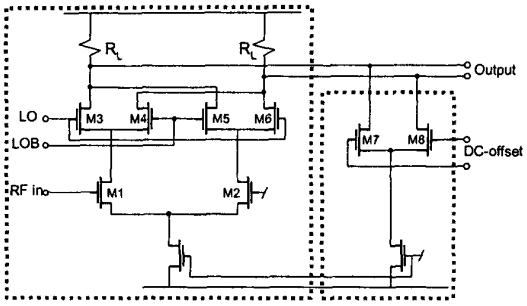

Figure 6. Circuit schematic of down-conversion mixer and dc-offset cancellation circuit

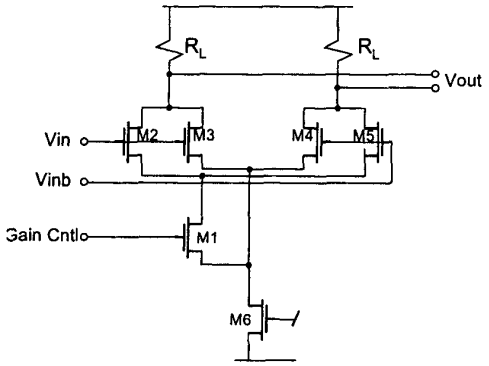

Figure 7 Circuit schematic of baseband variable gain amplifier

In addition to the RFI-transceiver, we have designed digital baseband circuitry to permit functional testing of RFI as shown in Fig. 5. The data source in the transmitter can generate either binary (2-PAM) or 3-level (3-PAM) data depending on the mode selection. The 3-PAM signaling is intended for demonstrating the RFI's potential in multi-level signal transmission. The two bits (UB/LB) fixed patterns from the data source correspond to 1010/1010 for 2-PAM and 1000/1010 for 3-PAM. A current-switch type DAC adds the UB/LB to yield the 2-PAM or 3-PAM data. In the receiver, the baseband signal is recovered by two dynamic comparators with reference voltages of V_{refH} and V_{refL} in 3-PAM mode or a common V_{ref} in 2-PAM mode, as shown in the inset of Fig. 5.

A prototype transceiver is fabricated in 0.18-μm 1-poly 6-metal CMOS. A chip micrograph is shown in Fig. 8. The length of the interconnect line between the transmitter and receiver is about 0.5mm. The total transmitter and the receiver consume chip areas of 220×150 μm^2 and 330×170 μm^2, respectively, while the RF-transceiver takes only 300×140 μm^2.

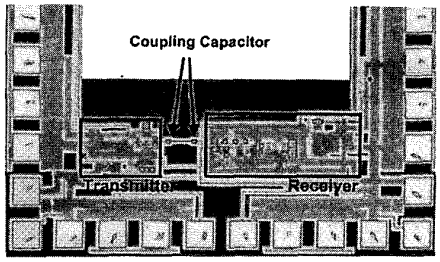

Figure 8. Chip micrograph

IV. MEASUREMENT RESULTS

The chip is tested on-wafer using a high frequency probe card. Fig. 9 shows the measurement setup for RFI testing. The 10.5-GHz 0.3-Vp LO is supplied externally and a phase shifter is used to correct the phase difference. The RF-transceiver consumes 9.5 mA from a 2.0V supply.

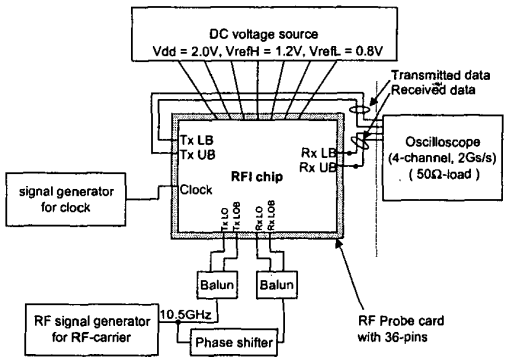

Figure 9. Measurement setup for RFI testing

Fig. 10 shows the measurement results for 2-PAM mode transmission with 2-GHz clock. The data rate is 2-Gb/s. The transmitted (Tx UB) and received (Rx UB) data are shown together. Rx UB is measured with RF LO turned on and off, where it is clearly shown that no signal is detected without RF LO. It indicates the RFI is operational with the RF-modulation and the capacitive coupling.

The operation modes are switched between 3-PAM and 2-PAM with a periodic pulse applied to the mode selection. Fig. 11 shows measurement results for the received data in addition to the simulated waveforms for the mode selection (Mode), the transmitted data (Tx UB/LB), the modulated signal on the channel (Channel), and the received data (Rx UB/LB). It shows that the data is successfully transmitted without error. With a 1.1GHz clock, the aggregate data rate of 2.2 Gb/s is achieved for both channels (UB/LB). In the

same way, data transmission at a lower clock rate is also measured. Fig. 12 shows the measured output waveforms at 800-MHz clock, which results in 1.6 Gb/s data rate. Note that the effective signaling level in 3-PAM mode is only half of 2-PAM mode (0.1V). It implies that this RFI can be extended to handle 4-PAM signal once with a full implementation of 2-bit DAC and ADC.

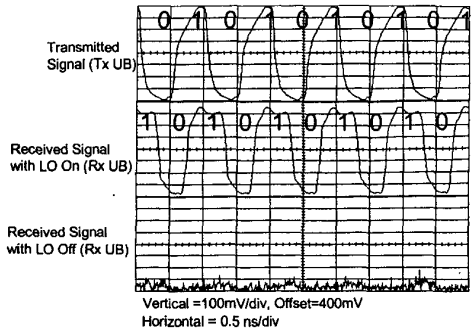

Figure 10. Measured output waveforms with f_{clk}=2GHz

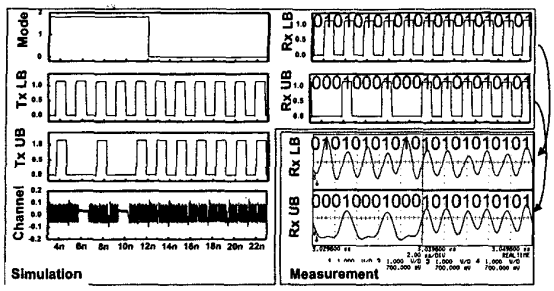

Figure 11. Measured/simulated waveforms for two channels (UB, LB) with f_{clk}=1.1GHz and aggregate data rate=2.2Gbps. Also shown are the mode selection signal and the modulated signal on the channel.

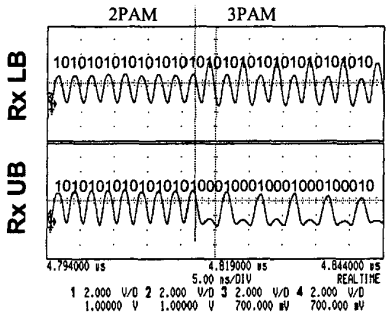

Figure 12. Measured output waveforms with f_{clk}=0.8GHz and aggregate data rate=1.6Gbps

V. RFI ADVANTAGES OVER DCI

Table I summarizes the major differences between RFI and DCI. A much smaller signal swing in RFI is enabled by the improved noise environment through: 1) 17.5-dB suppression of noise coupling into the channel; 2) no dc current dissipation on the channel; 3) silent GND termination, 4) lower switching current (8mA versus 30mA). The RF-circuit overhead for RFI is reduced by using the direct conversion transceiver architecture and can be further decreased, for instance, by incorporating time-division multiplexing for multiple I/Os.

Table I. System Advantages of RFI over DCI

	DCI	RFI
Transmission line	25-Ω matched termination	25-Ω matched termination
Termination voltage	Regulated Voltage	GND
Voltage swing at channel	0.8 V (+1.8V / +1.0V)	0.2 V (+0.1V / -0.1V)
Switching current from output driver	30 mA	± 4 mA
DC current on the channel	0 or 30 mA	0 mA
Output driver	Open drain with slew rate control	High-efficiency power amplifier with impedance matched load
Circuit overhead	DLL Slew rate control	RF PLL Direct conversion transceiver

VI. CONCLUSIONS

RFI enables enhanced signal-to-noise ratio, lower signal swing, lower switching noise, and lower output power consumption while increases the transmission data rate of the channel potentially up to the Nyquist speed of $f_{RF}/2$. We believe that the RFI can be very instrumental for high-speed link applications in multi-memory and microprocessor interfaces.

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